Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (*currently amended*) An image display system for synchronizing the display of images on a plurality of display devices, comprising:

a first computer system generating a first signal representing first image data to be displayed on a first display device;

a second computer system generating a second signal representing second image data to be displayed on a second display device; and

means for synchronizing said first and second image data, said synchronizing means comprising:

a master sync signal generated from a master sync signal generator; and

a signal generating means for receiving the master sync signal and generating a video clock signal from the master sync signal wherein the video clock signal is synchronized with the master sync signal;

a comparison means for determining if the video clock signal is no longer synchronized with the master sync signal;

wherein in response to the comparison means determining that the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal; and

wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, wherein the duration of the convergence time is programmable, said duration of the convergence time beginning at the start of convergence and ending at the achievement of convergence.

2–10. (*previously cancelled*).

11. *(original)* An apparatus for synchronizing to a first digital signal, generation of a second digital signal, comprising:

a phase detector for comparing the first digital signal to a comparison pulse stream to produce a difference pulse stream;

a low pass filter for filtering said difference pulse stream to produce an analog signal;

a voltage controlled oscillator for producing the second digital signal in response to the analog signal;

and a digital rate controller that divides the second digital signal by a divisor value to produce said comparison pulse stream, wherein said digital rate controller produces said divisor value based on a programmable rate value and a comparison of the first digital signal and said comparison pulse stream.

12. *(original)* A system for synchronizing video frame rate between a first video system displaying video images on a first display device and a second video system displaying video images on a second display device, the system comprising:

a master sync signal generator;

a first video input/output module associated with said first video system;

and a second video input/output module associated with said second video system,

wherein each of said video input/output modules comprises a sync separator that receives said master sync signal and produces a master pulse stream therefrom;

a phase detector that compares said master pulse stream to a slave pulse stream to produce a difference pulse stream;

a low pass filter that filters said difference pulse stream to produce an analog signal;

a voltage controlled oscillator that produces a video clock signal in response to said analog signal;

and a digital rate controller that divides said clock signal by a divisor value to produce said slave pulse stream, said digital rate controller producing said divisor value

based on a programmable rate value and a comparison of said master pulse stream and said slave pulse stream.

13. *(original)* The system of claim 12, wherein said video input/output modules further comprise: a video generator to generate a video signal in response to said clock signal.

14. (*previously presented*) The image display system of claim 1, wherein the signal generating means comprises a video input/output module comprised of a phase-locked loop circuit and a programmable digital rate controller;

wherein the phase-locked loop circuit generates the video clock signal;

wherein the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal;

wherein the comparison means comprises the programmable digital rate controller, said programmable digital rate controller determining if the video clock signal is no longer synchronized with the master sync signal; and

wherein the programmable digital rate controller further controls a lock responsiveness rate at which the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal, wherein a faster lock responsiveness rate results in a shorter convergence time and a slower lock responsiveness rate results in a longer convergence time.

15. (*previously presented*) The image display system of claim 14, wherein the video input/output module further comprises a sync separator for receiving the master sync signal and extracting a master pulse stream from the master sync signal.

16. (*previously presented*) The image display system of claim 15, wherein the phase-locked loop circuit is comprised of:

a phase detector for comparing the received master pulse stream to a received slave pulse stream to produce a difference pulse stream, wherein the width of a

difference pulse in the difference pulse stream represents a difference between the master pulse stream and the slave pulse stream;

a low pass filter for filtering the difference pulse stream to produce an analog signal; and

a voltage controlled oscillator for generating the video clock signal in response to the analog signal.

17. (*currently amended*) The image display system of claim 16, wherein the programmable digital rate controller receives the video clock signal; ~~and~~

wherein the programmable digital rate controller divides the video clock signal by a divisor value to produce the slave pulse stream; and

wherein the programmable digital rate controller generates the divisor value based on a programmable lock speed and a comparison of the master pulse stream and the slave pulse stream.

18. (*previously presented*) The image display system of claim 17, wherein the programmable digital rate controller is comprised of a digital comparator, a rate controller, and a programmable divider;

wherein the digital comparator generates a lead/lag difference signal by comparing the master pulse stream and the slave pulse stream;

wherein the rate controller generates the divisor value based on the lead/lag difference signal and the programmable lock speed; and

wherein the programmable divider divides the video clock signal by the divisor value to produce the slave pulse stream by generating an output pulse in the slave pulse stream, wherein the output pulse is generated each time the programmable divider counts off a number of pulses in the video clock signal, the number of pulses being equal to the divisor value.

19. (*previously presented*) The image display system of claim 14, wherein the first and second image data comprise respective video images processed by a respective first video input/output module of the first computer system and a respective second video input/output module of the second computer system.

20. (*previously presented*) The image display system of claim 19, wherein the video input/output module further comprises a video generator for generating a video signal in response to the video clock signal which is synchronized to the master sync signal.

21. (*previously presented*) The image display system of claim 14, wherein each of the first image data and the second image data comprises a respective computer graphics image.

22. (*previously presented*) The image display system of claim 21, wherein each of the first and second computer systems further comprises a respective graphics processor for generating the respective computer graphics image.

23. (*previously presented*) The image display system of claim 22, wherein each graphics processor generates the computer graphics image in response to the video clock signal which is synchronized to the master sync signal.

24. (*previously presented*) The image display system of claim 1,

wherein the signal generating means comprises a video input/output module;

wherein the first computer system comprises a first video input/output module and the second computer system comprises a second video input/output module;

wherein the first video input/output module and the second video input/output module receive the master sync signal from the master sync signal generator; and

wherein the master sync signal generator is external to the first computer system and the second computer system.

25. (*previously presented*) The image display system of claim 1,

wherein the signal generating means comprises a video input/output module;

wherein the first computer system comprises the master sync signal generator;

wherein the second computer system comprises the video input/output module; and

wherein the video input/output module synchronizes to the master sync signal received from the master sync signal generator;

wherein the first computer system is a master computer system and the second computer system is a slave display system.

26. (*previously presented*) The image display system of claim 25, wherein the master sync signal is generated from a graphics processor of the master computer system.

27. (*new*) An image display system for synchronizing the display of images on a plurality of display devices, comprising:

a first computer system generating a first signal representing first image data to be displayed on a first display device;

a second computer system generating a second signal representing second image data to be displayed on a second display device; and

means for synchronizing said first and second image data, said synchronizing means comprising:

a master sync signal generated from a master sync signal generator; and

a signal generating means for receiving the master sync signal and generating a video clock signal from the master sync signal wherein the video clock signal is synchronized with the master sync signal;

a comparison means for determining if the video clock signal is no longer synchronized with the master sync signal;

wherein in response to the comparison means determining that the video clock signal is no longer synchronized with the master sync signal, the signal generating means

reestablishes the synchronization between the video clock signal and the master sync signal; and

wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a programmable convergence time, such that a speed of the convergence of the video clock signal and the master sync signal is thereby programmably adjustable.

28. (*new*) The image display system of claim 27, wherein the signal generating means comprises a video input/output module comprised of a phase-locked loop circuit and a programmable digital rate controller;

wherein the phase-locked loop circuit generates the video clock signal;

wherein the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal;

wherein the comparison element comprises the programmable digital rate controller, said programmable digital rate controller determining if the video clock signal is no longer synchronized with the master sync signal; and

wherein the programmable digital rate controller further controls a lock responsiveness rate at which the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal, wherein:

a faster lock responsiveness rate results in a faster speed of the convergence;

and a slower lock responsiveness rate results in a slower speed of the convergence.

29. (*new*) The image display system of claim 28, wherein the video input/output module further comprises a sync separator for receiving the master sync signal and extracting a master pulse stream from the master sync signal.

30. (*new*) The image display system of claim 29, wherein the phase-locked loop circuit is comprised of:

a phase detector for comparing the received master pulse stream to a received slave pulse stream to produce a difference pulse stream, wherein the width of a difference pulse in the difference pulse stream represents a difference between the master pulse stream and the slave pulse stream;

a low pass filter for filtering the difference pulse stream to produce an analog signal; and

a voltage controlled oscillator for generating the video clock signal in response to the analog signal.

31. (*new*) The image display system of claim 30, wherein the programmable digital rate controller receives the video clock signal;

wherein the programmable digital rate controller divides the video clock signal by a divisor value to produce the slave pulse stream; and

wherein the programmable digital rate controller generates the divisor value based on a programmable lock speed and a comparison of the master pulse stream and the slave pulse stream.

32. (*new*) The image display system of claim 30, wherein the programmable digital rate controller is comprised of a digital comparator, a rate controller, and a programmable divider;

wherein the digital comparator generates a lead/lag difference signal by comparing the master pulse stream and the slave pulse stream;

wherein the rate controller generates the divisor value based on the lead/lag difference signal and the programmable lock speed; and

wherein the programmable divider divides the video clock signal by the divisor value to produce the slave pulse stream by generating an output pulse in the slave pulse stream, wherein the output pulse is generated each time the programmable divider counts off a number of pulses in the video clock signal, the number of pulses being equal to the divisor value.